Claims

1. Data link layer device for a serial communication bus, in particular IEEE1394 bus, comprising an interface (35) to a physical layer unit (20) and an interface (36) to at least one host processor supporting the higher layers of the OSI/ISO data communication reference model, further comprising a counter (31a) counting clock pulses of a reference clock, the counter (31a) generating a cycle synchronization event each time after a predetermined counting interval, the cycle synchronization event triggering the generation and submission of a cycle start packet by means of a packet transmitter (32) for time synchronization of the bus station, **characterized in that**, the data link layer unit further comprises configuration means (31b, 38) with which the generation and submission of a cycle start packet in succession to a cycle synchronization event are disabled in response to a predetermined condition in order to support a no cycle master transfer mode.

2. Data link layer device according to claim 1, wherein the configuration means (31b, 38) comprise means for requesting from an isochronous resource manager (42) whether bandwidth has been allocated for isochronous data transfers, and the configuration means (31b, 38) disabling said generation and submission of the cycle start packet if no bandwidth allocation for isochronous data transfers has been made.

3. Data link layer device for a serial communication bus, in particular IEEE1394 bus, comprising an interface (35) to a physical layer unit (20) and an interface to at least one host processor supporting the higher layers of the OSI/ISO data communication reference model, **characterized in that**, a data link layer device further comprises means

(31b) for checking whether a cycle master exists in the network and if not activating configuration means (38) that enable the generation of asynchronous transmission requests without waiting for a cycle start packet and an isochronous data transfer in order to support a no cycle master transfer mode.

4. Data link layer device according to claim 3 wherein the means for checking whether a cycle master exists in the network comprise a memory (37) storing the self-identification packets from all the nodes in the network and evaluating means for checking whether in one of the self-identification packets an entry is found that indicated that the corresponding node is contender for an isochronous resource manager (42).

5. Data link layer device according to claim 3, wherein the means for checking whether a cycle master exists in the network comprise a first counter (31a) counting clock pulses of a reference clock, the counter generating a cycle synchronization event each time after a predetermined counting interval, and comprising a second counter that is incremented each time that no cycle start packet has been received in succession to a cycle synchronization event, thereby activating said configuration means if the second counter reaches a predetermined value.